L Number	Hits	Search Text	DB	Time stamp
•	1	5437034.pn.	USPAT	2003/12/30 13:01
-	1	6226776.pn.	USPAT	2003/12/19 17:30
-	1	5600579.pn.	USPAT	2003/12/19 17:30
-	1	5774380.pn.	USPAT	2003/12/19 17:31
-	11	("5437034" US-6226776 US-5600579 US-5774380) and (HDL	USPAT	2003/12/27 22:37
		VHDL system simulation simulating simulate circuit model code		
		coded coding storing store stored saved save saving recording		
		record recorded executed hardware description language object		
	200	code "C" programming program programmed)	LICDAT	2004/01/02 10:50
-	208	(HDL VHDL "hardware description language" ) and system and	USPAT	2004/01/03 18:59
		(simulation simulating simulate) and circuit and model and (code		
		coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and		
	74	(programming program programmed) (HDL VHDL "hardware description language" ) and system and	USPAT	2003/12/27 22:40
-	/4	(simulation simulating simulate) and circuit and model and (code	USPAT	2003/12/27 22.40
		coded coding) and (storing store stored saved save saving		
		recording record recorded) and executed and object and "C" and		
		(programming program programmed) and @pd < "19990930"		
_	74	(HDL VHDL "hardware description language" ) and system and	USPAT;	2003/12/27 22:40
_	77	(simulation simulating simulate) and circuit and model and (code	US-PGPUB;	2003/12/27 22.10
		coded coding) and (storing store stored saved save saving	EPO; JPO;	
		recording record recorded) and executed and object and "C" and	DERWENT;	
		(programming program programmed) and @pd < "19990930"	IBM_TDB	
_	62	(HDL VHDL "hardware description language" ) and system and	USPAT;	2003/12/27 22:42
-	02	(simulation simulating simulate) and circuit and model and (code	US-PGPUB;	2000, 22, 22, 12
		coded coding) and (storing store stored saved save saving	EPO; JPO;	
		recording record recorded) and executed and object and "C" and	DERWENT;	
		(programming program programmed) and @pd < "19990930" and	IBM_TDB	
		(convert converting converted compile compiling compiled)		
-	58	(HDL VHDL "hardware description language" ) and system and	USPAT;	2003/12/27 22:43
		(simulation simulating simulate) and circuit and model and (code	US-PGPUB;	
		coded coding) and (storing store stored saved save saving	EPO; JPO;	
		recording record recorded) and executed and object and "C" and	DERWENT;	
		(programming program programmed) and @pd < "19990930" and	IBM_TDB	
		(convert converting converted compile compiling compiled) and		
		(clock clocking clocked cycle cycling)		
-	<del>4</del> 9	(HDL VHDL "hardware description language" ) and system and	USPAT;	2003/12/27 22:44
		(simulation simulating simulate) and circuit and model and (code	US-PGPUB;	
		coded coding) and (storing store stored saved save saving	EPO; JPO;	
		recording record recorded) and executed and object and "C" and	DERWENT;	
		(programming program programmed) and @pd < "19990930" and	IBM_TDB	
		(convert converting converted compile compiling compiled) and		
		(clock clocking clocked cycle cycling) and (binary digital "0/1"		
	40	"1/0" assembling)	LICDAT.	2003/12/27 22:45
-	49	(HDL VHDL "hardware description language") and system and	USPAT; US-PGPUB;	2003/12/27 22.43
		(simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving	EPO; JPO;	
		recording record recorded) and executed and object and "C" and	DERWENT;	
		(programming program programmed) and @pd < "19990930" and	IBM_TDB	
		(convert converting converted compile compiling compiled) and	1914_100	
		(clock clocking clocked cycle cycling) and (binary digital "0/1"		
		"1/0" assembling) and (CPU processor microprocessor controller		
		calculation calculating calculated)		
	49		USPAT;	2003/12/31 00:08
		(simulation simulating simulate) and circuit and model and (code	US-PGPUB;	
		coded coding) and (storing store stored saved save saving	EPO; JPO;	
		recording record recorded) and executed and object and "C" and	DERWENT;	
		(programming program programmed) and @pd < "19990930" and	IBM_TDB	
		(convert converting converted compile compiling compiled) and	1	
		(clock clocking clocked cycle cycling) and (binary digital "0/1"		
		"1/0" assembling) and (CPU processor microprocessor controller		
		calculation calculating calculated) and object		

(simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and (clock clocking clocked cycle cycling) and (binary digital "0,1" "1,0" assembling) and (CPU processor microprocessor controller calculation calculating calculated) and object and (PLI "programming language interface") PT "4) PLI "Programming language interface" PAT "application programming interface") PT (HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved saves saving recording record recorded) and executed and object and "C" and (programming program programmed) and @pd < "19999930" and (clock clocking clocked cycle cycling) and (binary digital "0,1" "1,0" assembling) and (CPU processor microprocessor controller calculation calculating calculated) and object and (PLI "programming language interface") PH "application programming interface" PH "Application programming interface") PH					
(HDL WHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "c" and (programming program programmed) and @pd < "19990930" and (convert converting converted compile compiling compiled) and (clock clocking clocked cycle cycling) and (binary digital "0/1" "1/0" assembling) and (ZPU processor microprocessor controller calculation calculating calculated) and object and (PLI "programming language interface" API "application programming interface")  7 (HDL WHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and @pd < "19990930" and (clock clocking clocked cycle cycling) and (binary digital "0/1" "1/0" assembling) and (CPU processor microprocessor controller calculation calculating calculated) and object and (PLI "programming language interface" API "application programming interface")  9 (HDL WHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and @pd < "1999030" and (convert converting complece compling complied) and (convert converting complece compling complied) and (convert converting complece compling complied) and (clock clocking clocked cycle cycling) and (binary digital "0/1" "1/0" assembling) auguage interface" API "application programming interface")  10 ("convert" complie") adi "HDL" adi "to" adi "binary"  11 ("convert" complie") adi "HDL" same code and @ad < USPAT 2003/12/28 21:16 2003/12/28 21:16 2003/12/28 21:16 2003/12/28 21:16 2003/12/28 21:16 2003/12/28 21:16 2003/12/28 21:16 2003/12/28 21:16 2003		7	(simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and @pd < "19990930" and (convert converting converted compile compiling compiled) and (clock clocking clocked cycle cycling) and (binary digital "0/1" "1/0" assembling) and (CPU processor microprocessor controller calculation calculating calculated) and object and (PLI "programming language interface" API "application programming	US-PGPUB; EPO; JPO; DERWENT;	2003/12/27 22:49
(HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and @pd < "19990930" and (convert converting converted compile compiling compiled) and (clock clocking clocked cycle cycling) and (binary digital "0/1" "1/0" assembling) and (CPU processor microprocessor controller calculation calculating calculated) and object and (PLI "programming language interface" API "application programming interface")  9 (HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and @pd < "19990930" and (convert converting converted compile compiling compiled) and (clock clocking clocked cycle cycling) and (binary digital "0/1" "1/0" assembling) and (CPU processor microprocessor controller calculation calculation calculated) and object and (PLI "programming language interface" API "application programming interface")  4 (US-5600579-\$ or US-5437034-\$ or US-6226776-\$ or US-5774380-\$).did.  2 "60156732" "60/156,732" "60,156,732" USPAT US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT USPAT USPAT USPAT 2003/12/28 21:10 ("convert" "compile") adj "HDL" same "binary" USPAT USPAT 2003/12/28 21:10 ("convert" "compile") adj "HDL" same code uSPAT 2003/12/28 21:11 ("convert" "compile") adj "HDL" same code and @ad < USPAT 2003/12/28 21:33 "19990930"  0 ("convert" "compile") adj "HDL" same binary and @pd < USPAT 2003/12/28 21:36 "19990930"  1 ("convert" "compile") adj "HDL" same binary and @pd < USPAT 2003/12/28 21:36 "19990930"  2 ("convert" "compile") adj "HDL" same binary and @ad < USPAT 2003/12/28 21:36 "19990930"	-	7	(HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and @pd < "1999030" and (convert converting converted compile compiling compiled) and (clock clocking clocked cycle cycling) and (binary digital "0/1" "1/0" assembling) and (CPU processor microprocessor controller calculation calculating calculated) and object and (PLI "programming language interface" API "application programming	USPAT	2003/12/27 22:54
HDL VHDL "hardware description language" ) and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and @pd < "19990930" and (convert converting converted compile compiling compiled) and (clock clocking clocked cycle cycling) and (binary digital "0/1" "1/0" assembling) and (CPU processor microprocessor controller calculation calculating calculated) and object and (PLI "programming language interface" API "application programming interface")   USPAT	-	7	(HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and @pd < "19990930" and (convert converting converted compile compiling compiled) and (clock clocking clocked cycle cycling) and (binary digital "0/1" "1/0" assembling) and (CPU processor microprocessor controller calculation calculating calculated) and object and (PLI "programming language interface" API "application programming	USPAT	2003/12/27 22:55
- 4 (US-5600579-\$ or US-5437034-\$ or US-6226776-\$ or US-5774380-\$).did 2 "60156732" "60/156,732" "60,156,732"  - 0 ("convert" "compile") adj "HDL" adj "to" adj "binary" - 58 ("convert" "compile") adj "HDL" - 0 ("convert" "compile") adj "HDL" - 10 ("convert" "compile") adj "HDL" - 22 ("convert" "compile") adj "HDL" same "binary" - 22 ("convert" "compile") adj "HDL" same code - 18 ("convert" "compile") adj "HDL" same code and @ad < USPAT 2003/12/28 21:37 - 19990930" - 0 ("convert" "compile") adj "HDL" same binary and @pd < USPAT 2003/12/28 21:38 - 19990930" - 10 ("convert" "compile") adj "HDL" same binary and @ad < USPAT 2003/12/28 21:38 - 2003/12/28 21:38		9	(HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and @pd < "19990930" and (convert converting converted compile compiling compiled) and (clock clocking clocked cycle cycling) and (binary digital "0/1" "1/0" assembling) and (CPU processor microprocessor controller calculation calculating calculated) and object and (PLI "programming language interface" API "application programming	USPAT	2003/12/28 21:46
- 2 "60156732" "60/156,732" "60,156,732"  USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB  ("convert" "compile") adj "HDL" adj "to" adj "binary"  USPAT 2003/12/28 21:10  USPAT 2003/12/28 21:37  USPAT 2003/12/28 21:38  "19990930"  USPAT 2003/12/28 21:38  "19990930"  USPAT 2003/12/28 21:38  "19990930"  USPAT 2003/12/28 21:38  "19990930"  USPAT 2003/12/28 21:38	-	4	(US-5600579-\$ or US-5437034-\$ or US-6226776-\$ or	USPAT	2003/12/27 22:59
- 58 ("convert" "compile") adj "HDL" USPAT 2003/12/28 21:10 - 0 ("convert" "compile") adj "HDL" same "binary" USPAT 2003/12/28 21:10 - 22 ("convert" "compile") adj "HDL" same code USPAT 2003/12/28 21:11 - 18 ("convert" "compile") adj "HDL" same code and @ad < USPAT 2003/12/28 21:37 - 19990930" - 0 ("convert" "compile") adj "HDL" same binary and @pd < USPAT 2003/12/28 21:38 - 19990930" - 0 ("convert" "compile") adj "HDL" same binary and @ad < USPAT 2003/12/28 21:38 - 19990930" - 2 ("convert" "compile") adj "HDL" same machine and @ad < USPAT 2003/12/28 21:45	-	2	"60156732" "60/156,732" "60,156,732"	US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/27 23:00
- 0 ("convert" "compile") adj "HDL" same "binary" USPAT 2003/12/28 21:10 - 22 ("convert" "compile") adj "HDL" same code USPAT 2003/12/28 21:11 - 18 ("convert" "compile") adj "HDL" same code and @ad < USPAT 2003/12/28 21:37 - 19990930" - 0 ("convert" "compile") adj "HDL" same binary and @pd < USPAT 2003/12/28 21:38 - "19990930" - 0 ("convert" "compile") adj "HDL" same binary and @ad < USPAT 2003/12/28 21:38 - "19990930" - 2 ("convert" "compile") adj "HDL" same machine and @ad < USPAT 2003/12/28 21:45	-	1			2003/12/28 21:10
- 22 ("convert" "compile") adj "HDL" same code 18 ("convert" "compile") adj "HDL" same code and @ad < USPAT 2003/12/28 21:37 19990930" - 0 ("convert" "compile") adj "HDL" same binary and @pd < USPAT 2003/12/28 21:38 19990930" - 0 ("convert" "compile") adj "HDL" same binary and @ad < USPAT 2003/12/28 21:38 19990930" - 2 ("convert" "compile") adj "HDL" same machine and @ad < USPAT 2003/12/28 21:45	-	1 _ 1			2003/12/28 21:10
'19990930"	-	1	("convert" "compile") adj "HDL" same code	USPAT	2003/12/28 21:11
"19990930"	-	18		USPAT	2003/12/28 21:37   
"19990930"	-	0		USPAT	2003/12/28 21:38
	-	0		USPAT	2003/12/28 21:38
	-	2		USPAT	2003/12/28 21:45

-	1	("convert" "compile") adj "HDL" same machine and @pd < "19990930"	USPAT	2003/12/28 21:45
-	9	(HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and @pd < "19990930" and (convert converting converted compile compiling compiled) and (clock clocking clocked cycle cycling) and (binary digital "0/1" "1/0" assembling) and (CPU processor microprocessor controller calculation calculating calculated) and object and (PLI "programming language interface" API "application programming interface")	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/28 21:47
	9	(HDL VHDL "hardware description language" ) and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and @pd < "19990930" and (clock clocking clocked cycle cycling) and (binary digital "0/1" "1/0" assembling) and (CPU processor microprocessor controller calculation calculating calculated) and object and (PLI "programming language interface" API "application programming interface") and (convert converting converted compile compiling compiled) same (machine code binary assembly)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/28 21:55
-	4	(HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and @pd < "19990930" and (clock clocking clocked cycle cycling) and (binary digital "0/1" "1/0" assembling) and (CPU processor microprocessor controller calculation calculating calculated) and object and (PLI "programming language interface" API "application programming interface") and (convert converting converted compile compiling compiled) adj4 (code binary assembly)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/28 22:08
-	9	(HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and @pd < "19990930" and (clock clocking clocked cycle cycling) and (binary digital "0/1" "1/0" assembling) and (CPU processor microprocessor controller calculation calculating calculated) and object and (PLI "programming language interface" API "application programming interface") and (convert converting converted compile compiling	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/29 13:56
-	1	compiled compiler compilers) and (code binary assembly machine) (HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and @pd < "19980930" and (clock clocking clocked cycle cycling) and (binary digital "0/1" "1/0" assembling) and (CPU processor microprocessor controller calculation calculating calculated) and object and (PLI "programming language interface" API "application programming interface") and (convert converting converted compile compiling	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/12/29 13:57
-	0	compiled compiler compilers) and (code binary assembly machine) (HDL VHDL "hardware description language") and system and (simulation simulating simulate) and circuit and model and (code coded coding) and (storing store stored saved save saving recording record recorded) and executed and object and "C" and (programming program programmed) and 5437037.pn.	USPAT	2003/12/30 13:02

-	0	(HDL VHDL "hardware description language" ) and system and	USPAT	2003/12/30 13:03
		(simulation simulating simulate) and circuit and model and (code		
		coded coding) and executed and object and "C" and		
1		(programming program programmed) and 5437037.pn.		
			LICDAT	2002/42/20 42:00
-	0	(HDL VHDL "hardware description language" ) and system and	USPAT	2003/12/30 13:03
		(simulation simulating simulate) and circuit and model and (code		
1		coded coding) and "C" and (programming program programmed)		
		and 5437037.pn.		
<u>-</u>	1	(HDL VHDL "hardware description language" ) and system and	USPAT	2003/12/31 00:33
	-	(simulation simulating simulate) and circuit and model and	00.711	2000, 12, 01 00.00
		(programming program programmed) and 5437037.pn.		2000/12/21
-	28	(HDL VHDL "hardware description language" ) and system and	USPAT;	2003/12/31 00:09
		(simulation simulating simulate) and circuit and model and (code	US-PGPUB;	
		coded coding) and (storing store stored saved save saving	EPO; JPO;	
		recording record recorded) and executed and object and "C" and	DERWENT;	
		(programming program programmed) and @pd < "19980930" and	IBM_TDB	
		(convert converting converted compile compiling compiled) and	1011_100	
		(clock clocking clocked cycle cycling) and (binary digital "0/1"		
		"1/0" assembling) and (CPU processor microprocessor controller		
1		calculation calculating calculated) and object		
-	17	(HDL VHDL "hardware description language" ) and system and	USPAT;	2003/12/31 00:09
		(simulation simulating simulate) and circuit and model and (code	US-PGPUB;	
		coded coding) and (storing store stored saved save saving	EPO; JPO;	
		recording record recorded) and executed and object and "C" and	DERWENT;	
		(programming program programmed) and @pd < "19980930" and	IBM_TDB	
		(convert converting converted compile compiling compiled) and		
		(clock clocking clocked cycle cycling) and (binary digital "0/1"		
		"1/0" assembling) and (CPU processor microprocessor controller		
		calculation calculating calculated) and object and oriented		
_	o	(HDL VHDL "hardware description language" ) near4 (compile	USPAT	2003/12/31 00:35
-	"		UJFAT	2003/12/31 00.33
		compiled compiling convert converting converted convertion)		
		near4 (assembly assembled)		
-	13	(HDL VHDL "hardware description language" ) same (compile	USPAT	2003/12/31 00:36
		compiled compiling convert converting converted convertion)		
		same (assembly assemling assembled)		
_	13	(HDL VHDL "hardware description language" ) same (compile	USPAT	2003/12/31 00:36
	15	compiled compiling convert converting converted convertion)		
		same (assembly assembling assembled) and pd<19980930	LICDAT	2002/12/21 00:10
-	1	(HDL VHDL "hardware description language" ) same (compile	USPAT	2003/12/31 00:40
		compiled compiling convert converting converted convertion)		
		same (assembly assemling assembled) and @pd<19980930		
-	2	(HDL VHDL "hardware description language" ) same (compile	USPAT	2003/12/31 00:44
		compiled compiling convert converting converted convertion)		
		same (assembly assembling assembled) and @pd<19990930		
_	4	((HDL VHDL "hardware description language" ) same (compile	USPAT	2003/12/31 12:40
-			UJFAI	2003/12/31 12:40
		compiled compiling convert converting converted convertion)		
		same (binary assembly assembled) and		
		@pd<19990930) and (HDL VHDL hardware description language		
		compile compiling compiled compilation converting convert		
		converted convertion binary assembling assembly)		
_	380	"HDL" and "RTL"	USPAT	2003/12/31 12:40
	306	"HDL" same "RTL"	USPAT	2003/12/31 12:40
_				
-	141	"HDL" same "RTL" and ("binary" "assembly")	USPAT	2003/12/31 12:41
-	123	"HDL" same "RTL" and ("binary" "assembly") and interface	USPAT	2003/12/31 12:41
-	13	"HDL" same "RTL" and ("binary" "assembly") and interface and	USPAT	2003/12/31 13:50
		@pd< "19980930"		
-	9538	Meyer.in.	USPAT	2003/12/31 13:51
_	0	Stven adj4 Meyer	USPAT	2003/12/31 13:51
_	1	Steven adj4 Meyer	USPAT	2003/12/31 13:51
_				
-	147	(HDL VHDL "hardware description language" ) and system and	USPAT	2004/01/07 12:28
		(simulation simulating simulate) and circuit and model and (code		
		coded coding) and (storing store stored saved save saving	1	
		recording record recorded) and executed and object and "C" and		
		(programming program programmed) and procedur\$		
		4:30:48 PM Page 4		

	,		*	
-	106	(HDL VHDL "hardware description language" ) and system and	USPAT	2004/01/03 19:03
		(simulation simulating simulate) and circuit and model and (code		
		coded coding) and (storing store stored saved save saving		
		recording record recorded) and executed and object and "C" and		
		(programming program programmed) and procedur\$ and task\$		
		and block\$ and delay\$		
-	106	(HDL VHDL "hardware description language" ) and system and	USPAT	2004/01/03 20:13
	100	(simulation simulating simulate) and circuit and model and (code	031 X1	200 1/01/03 20:13
		coded coding) and (storing store stored saved save saving		
		recording record recorded) and executed and object and "C" and		
		(programming program programmed) and procedur\$ and task\$		
		and block\$ and delay\$ and control\$ and (operation process)		
-	22	(HDL VHDL "hardware description language" ) and system and	USPAT	2004/01/03 20:24
		(simulation simulating simulate) and circuit and model and (code		
		coded coding) and (storing store stored saved save saving		
		recording record recorded) and executed and object and "C" and		
		(programming program programmed) and procedur\$ and task\$		
		and block\$ and delay\$ and control\$ and (operation process) and		
		@pd<19980930		0004/04/05 44 05
-	92	(HDL VHDL "hardware discription language" Verilog) and (PLI	USPAT;	2004/01/06 14:36
		"programming language interface")	US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
}			IBM TDB	
_	6	@pd < "19980930" and (HDL VHDL "hardware discription	USPAT;	2004/01/07 12:29
		language" Verilog) and (PLI "programming language interface")	US-PGPUB;	
		language verilog/ and (i as programming language interface )	EPO; JPO;	
			DERWENT;	
	_	O. L. WAGGGGGGGGGGGGGGGGGGGGGGGGGGGGGGGGGGGG	IBM_TDB	2004/04/05 44 40
-	5	@pd < "19980930" and (HDL VHDL "hardware discription	USPAT;	2004/01/06 14:40
		language" Verilog) and (PLI "programming language interface")	US-PGPUB;	
		and (C++ "C" "object-oriented language" "object oriented")	EPO; JPO;	
			DERWENT;	:
			IBM_TDB	
-	4	@pd < "19980930" and (HDL VHDL "hardware discription	USPAT;	2004/01/06 14:41
		language" Verilog) and (PLI "programming language interface")	US-PGPUB;	, ,
		and (C++ "C" "object-oriented language" "object oriented") and	EPO; JPO;	
		(simulation simulated simulate simulating) and (binary object code	DERWENT;	
		assembly)	IBM_TDB	
				2004/01/06 14:42
-	1	@pd < "19980930" and (HDL VHDL "hardware discription	USPAT;	2004/01/06 14:42
		language" Verilog) and (PLI "programming language interface")	US-PGPUB;	
		and (C++ "C" "object-oriented language" "object oriented") and	EPO; JPO;	
		(simulation simulated simulate simulating) and (binary assembly)	DERWENT;	
		and (object code)	IBM_TDB	
-	1	@pd < "19980930" and (HDL VHDL "hardware discription	USPAT;	2004/01/06 14:43
		language" Verilog) and (PLI "programming language interface")	US-PGPUB;	
		and (C++ "C" "object-oriented language" "object oriented") and	EPO; JPO;	
		(simulation simulated simulate simulating) and (binary assembly)	DERWENT;	
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_	1	@pd < "19980930" and (HDL VHDL "hardware discription	USPAT;	2004/01/06 14:43
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		language" Verilog) and (PLI "programming language interface")	US-PGPUB;	
		and (C++ "C" "object-oriented language" "object oriented") and	EPO; JPO;	
		(simulation simulated simulate simulating) and (binary assembly)	DERWENT;	
		and (memory stored storing storage)	IBM_TDB	
-	0	@pd < "19980930" and (HDL VHDL "hardware discription	USPAT;	2004/01/06 16:06
		language" Verilog) and (PLI "programming language interface")	US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
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-	22		USPAT	2004/01/07 12:29
		(simulation simulating simulate) and circuit and model and (code		
		coded coding) and (storing store stored saved save saving		
		recording record recorded) and executed and object and "C" and		
		(programming program programmed) and procedur\$ and (simulat\$ same binary)		
	1	[	USPAT;	2004/01/07 12:50
-	1	language" Verilog) and (PLI "programming language interface")	US-PGPUB;	2004/01/07 12.30
		and (simulat\$ same binary)	EPO; JPO;	
		and (simulacy same binary)	DERWENT;	
			IBM_TDB	
_	o	(binary assembly) same "all simulator"	USPAT;	2004/01/07 12:52
		(	US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	
-	0	(binary assembly) same "all simulators"	USPAT;	2004/01/07 12:52
			US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
	_		IBM_TDB	2004/04/07 42 52
-	0	(binary assembly) and "all simulators"	USPAT;	2004/01/07 12:52
			US-PGPUB;	
			EPO; JPO; DERWENT;	
			IBM_TDB	
	6653	(binary assembly) and simulator	USPAT;	2004/01/07 12:52
	0055	(billary assembly) and simulator	US-PGPUB;	2001/01/07 12:32
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	
-	3378	(binary assembly) and simulator and @pd < "19980930"	USPAT;	2004/01/07 12:53
			US-PGPUB;	
			EPO; JPO;	
	1		DERWENT;	
		//:   10000000  -m-	IBM_TDB	2004/01/07 12:54
-	0	(binary assembly) and simulator and @pd < "19980930" and	USPAT; US-PGPUB;	2004/01/07 12:54
		703/*.ccls	EPO; JPO;	
			DERWENT;	
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_	335	(binary assembly) and simulator and @pd < "19980930" and	USPAT;	2004/01/07 12:54
		"703"	US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
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-	0	(binary assembly) and simulator and @pd < "19980930" and	USPAT;	2004/01/07 12:55
		"703" and "all"	US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
		(binary assembly) and simulator and @pd < "19980930" and "all"	IBM_TDB USPAT;	2004/01/07 12:55
-	1	(minary assembly) and simulator and wha a tagonaso and an	US-PGPUB;	2007/01/07 12.55
			EPO; JPO;	
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